Figure 1: Cross Sectional View of Semiconductor Device

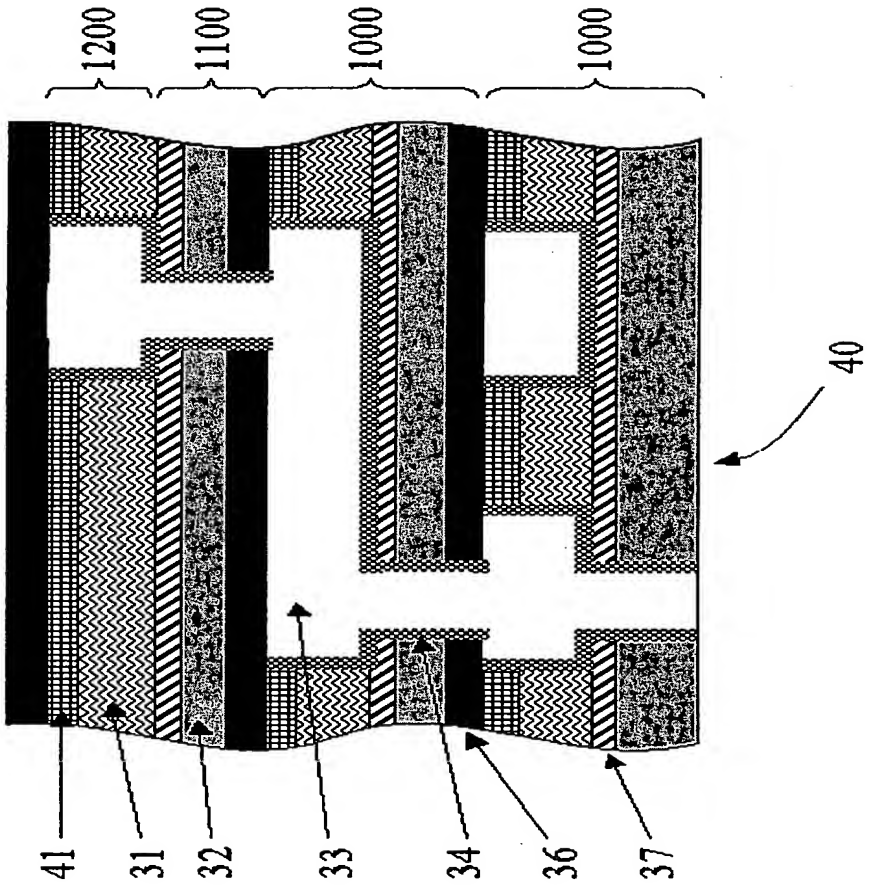

Figure 2: Cross Sectional View of Semiconductor Device

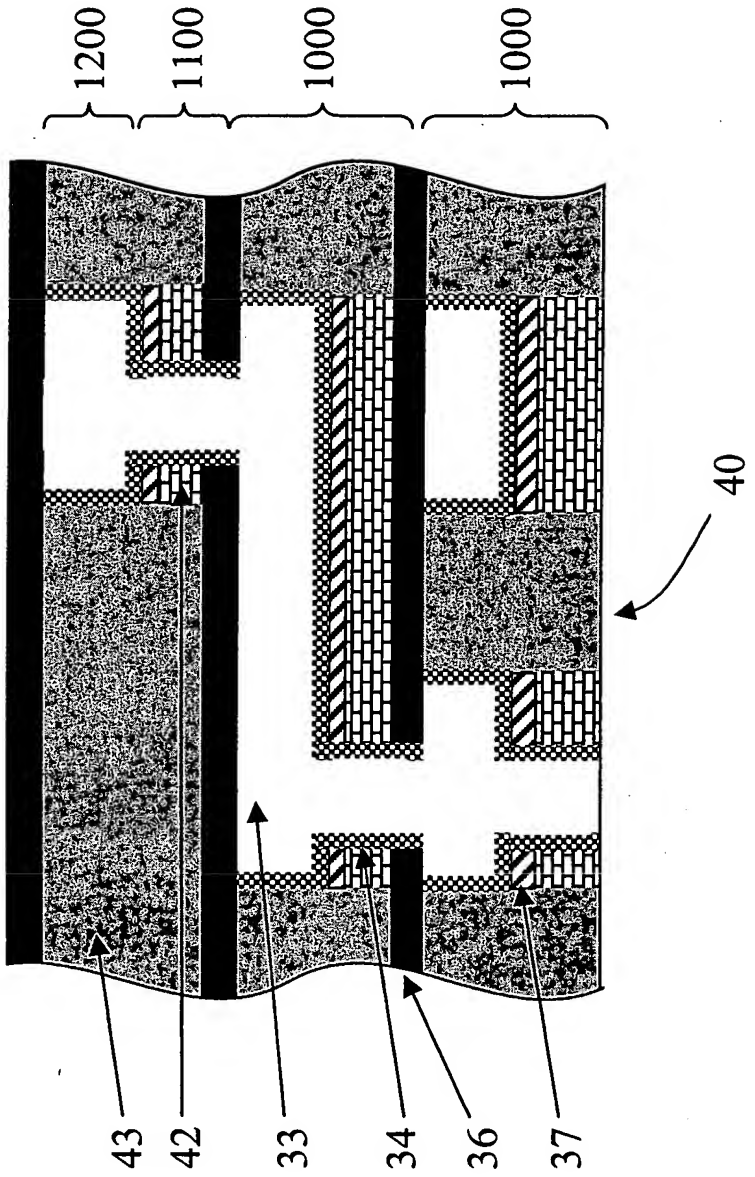

Figure 3: General Process Flow for Generation of Ceramic Diffusion Barrier Layer

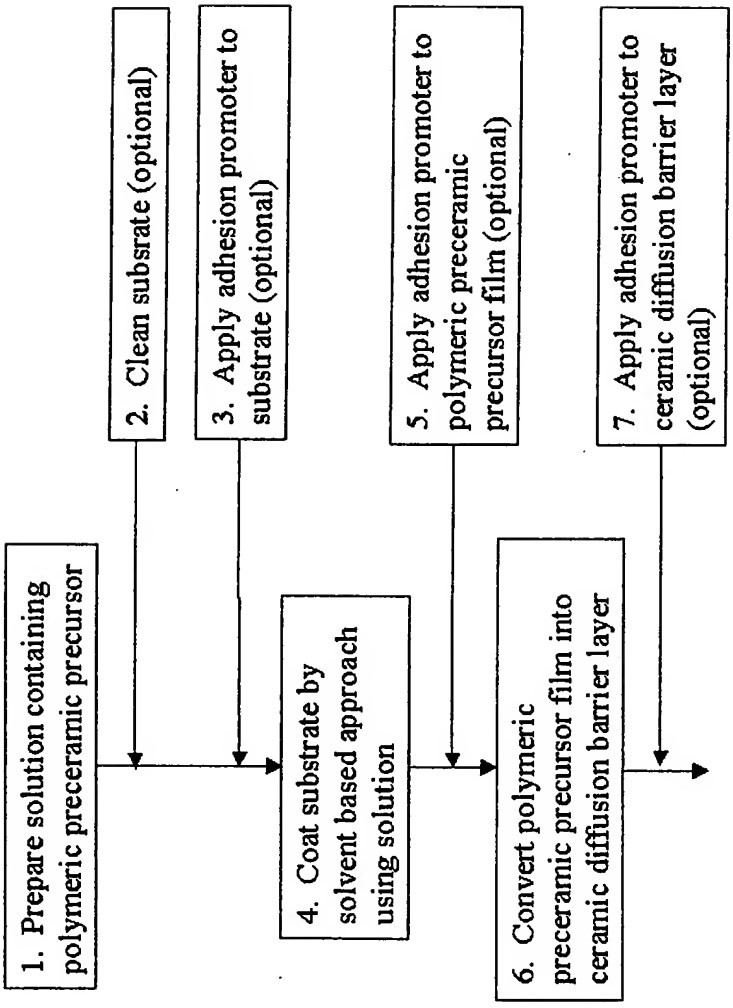

Figure 4: Electrical Data of Ceramic Diffusion Barrier Layer Generated from Polysilazane Polymer Preceramic Precursor

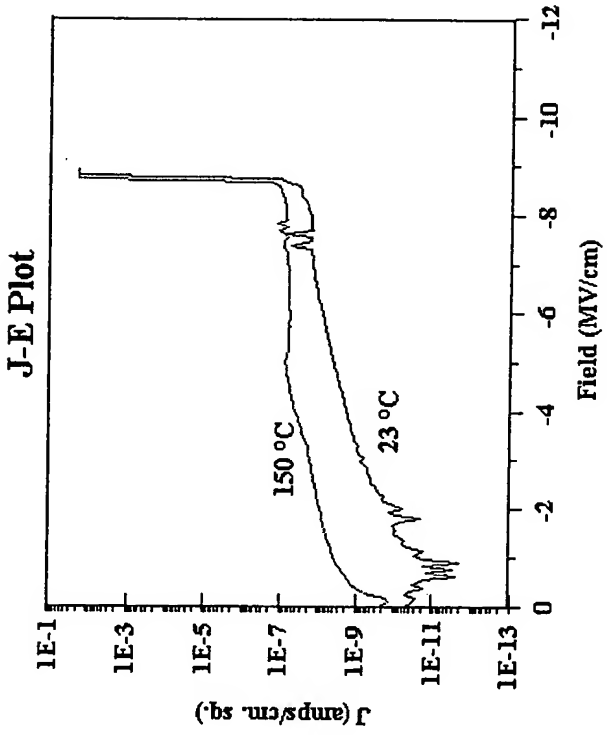

Fig. 4B

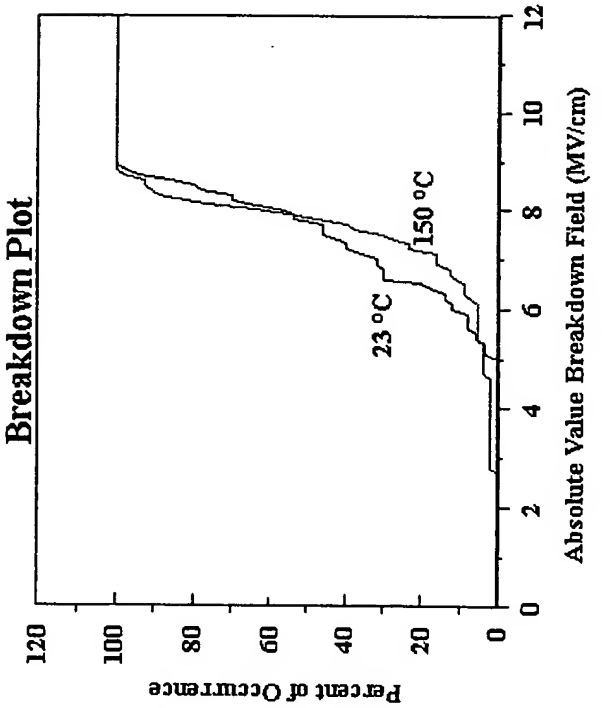

Fig. 4A